CLAIMS

[1] A clock input/output device comprising logic gates and operating as a gate that permits a clock to pass therethrough,

wherein the logic gates comprise:

a three-state inverter

of which a threshold voltage with reference to which the three-state inverter evaluates an input thereto to determine whether or not to change a state of an output thereof is equal to substantially one-half of a supply voltage fed in and

that switches the output thereof among three states, namely a high, a low, and a high-impedance state; and

an inverter

of which a threshold voltage with reference to which the inverter evaluates an input thereto to determine whether or not to change a state of an output thereof is equal to substantially one-half of the supply voltage fed in.

[2] The clock input/output device of claim 1,

wherein one of the logic gates is a two-input, one-output AND gate comprising:

a first three-state inverter

of which an input terminal serves as one input of the AND gate;

a second three-state inverter

of which an input terminal serves as another input of the AND gate

and

of which the input terminal is connected to a state control terminal thereof,

the second three-state inverter determining whether or not to bring an output thereof into a high-impedance state according to a state of a signal fed to the state control terminal thereof;

a first inverter

of which an input terminal is connected to a node between output terminals of the first and second three-state inverters, and

of which an output terminal serves as an output of the AND gate; and

a second inverter

of which an input terminal is connected to the input terminal of the second three-state inverter, and

of which an output terminal is connected to the state control terminal of the first three-state inverter,

wherein threshold voltages of the first and second three-state inverters and of the first and second inverters are substantially equal to one-half of the supply voltage fed in.

[3] The clock input/output device of claim 2,

wherein the first inverter is a three-state inverter of which a state control terminal is grounded.

[4] The clock input/output device of claim 1,

wherein one of the logic gates is a two-input, one-output OR gate comprising:

a first three-state inverter

of which an input terminal serves as one input of the OR gate, and

that receives at a state control terminal thereof another input to the OR gate ;

the first three-state inverter determining whether or not to bring an output thereof into a high-impedance state according to a state of a signal fed to the state control terminal thereof;

a second three-state inverter

of which an input terminal serves as another input of the OR gate;

a first inverter

of which an input terminal is connected to a node between output terminals of the first and second three-state inverters, and

of which an output terminal serves as an output of the OR gate; and

a second inverter

of which an input terminal is connected to the input terminal of the second three-state inverter, and

of which an output terminal is connected to the state control terminal of the second three-state inverter,

wherein threshold voltages of the first and second three-state inverters and of the first and second inverters are substantially equal to one-half of the supply voltage fed in.

[5] The clock input/output device of claim 3,

wherein the first inverter is a three-state inverter of which a state control terminal is grounded.

[6] The clock input/output device of claim 1,

wherein one of the logic gates is a logic gate that selects and outputs one of two clocks according to a select signal fed thereto, the logic gate comprising:

a first three-state inverter

that receives at an input terminal thereof one clock, and

that receives at a state control terminal thereof the select signal,

the first three-state inverter determining whether or not to bring an output thereof into a high-impedance state according to a signal fed to the state control terminal thereof;

a second three-state inverter

that receives at an input terminal thereof another clock;

a first inverter

of which an input terminal is connected to a node between output terminals of the first and second three-state inverters, and

of which an output terminal serves as an output of the logic gate; and

a second inverter

that receives at an input terminal thereof the select signal, and

of which an output terminal is connected to the state control terminal of the second three-state inverter,

wherein threshold voltages of the first and second three-state inverters and of the first and second inverters are substantially equal to one-half of the supply voltage fed in.

[7] The clock input/output device of claim 4,

wherein the first inverter is a three-state inverter of which a state control terminal is grounded.

[8] The clock input/output device of one of claims 1 to 7,

wherein the three-state inverter comprises:

a first transistor

that receives at a first electrode thereof the supply voltage;

a second transistor

of which a first electrode is connected to a second electrode of the first transistor, and

that is of a same conductivity type as the first transistor;

a third transistor

of which a second electrode is connected to a second electrode of the second transistor, and

that is of an opposite conductivity type to the first transistor;

a fourth transistor

of which a second electrode is connected to a first electrode of the third transistor,

of which a first electrode is grounded, and

that is of an opposite conductivity type to the first transistor; and

an inverter

of which an output terminal is connected to a control electrode of the third transistor,

wherein

a node between control electrodes of the first and fourth transistors serves as an input terminal of the three-state inverter,

a node between the second electrodes of the second and third transistors serves as an output terminal of the three-state inverter, and

a node between a control electrode of the second transistor and an input terminal of the inverter serves as a state control terminal of the three-state inverter.

[9] The clock input/output device of claim 1,

wherein an inverter provided in a last stage of the clock input/output device comprises:

a fifth transistor

that receives at a first electrode thereof the supply voltage, and

that is kept on during normal operation;

a sixth transistor

of which a first electrode is connected to a second electrode of the fifth transistor,

that receives at a control electrode thereof a clock outputted from a

logic gate provided in a previous stage, and

that is of a same conductivity type as the fifth transistor;

a seventh transistor

of which a second electrode is connected to a second electrode of the sixth transistor,

that receives at a control electrode thereof the clock outputted from the logic gate provided in the previous stage, and

that is of an opposite conductivity type to the fifth transistor; and

an eighth transistor

of which a second electrode is connected to a first electrode of the seventh transistor,

of which a first electrode is grounded,

that is kept on during normal operation, and

that is of an opposite conductivity type to the fifth transistor;

wherein a duty factor of a clock outputted from the clock input/output device is measured,

in a case where one end of a resistor of which another end is connected to a ground voltage is connected to a node between the second electrodes of the sixth and seventh transistors which serves as an output of the inverter, by measuring a current that flows through the resistor while the fifth transistor is kept on and the eighth transistor is kept off, and

in a case where one end of a resistor of which another end is connected to the supply voltage is connected to a node between

the second electrodes of the sixth and seventh transistors which serves as the output of the inverter, by measuring a current that flows through the resistor while the eighth transistor is kept on and the fifth transistor is kept off.

[10] A clock input/output device comprising logic gates and operating as a gate that permits a clock to pass therethrough,

wherein an inverter provided in a last stage of the clock input/output device comprises:

a first transistor

that receives at a first electrode thereof the supply voltage, and

that is kept on during normal operation;

a second transistor

of which a first electrode is connected to a second electrode of the first transistor,

that receives at a control electrode thereof a clock outputted from a logic gate provided in a previous stage, and

that is of a same conductivity type as the first transistor;

a third transistor

of which a second electrode is connected to a second electrode of the second transistor,

that receives at a control electrode thereof the clock outputted from the logic gate provided in the previous stage, and

that is of an opposite conductivity type to the first transistor; and

a fourth transistor

of which a second electrode is connected to a first electrode of the third transistor,

of which a first electrode is grounded,

that is kept on during normal operation, and

that is of an opposite conductivity type to the first transistor;

wherein a duty factor of a clock outputted from the clock input/output device is measured,

in a case where one end of a resistor of which another end is connected to a ground voltage is connected to a node between the second electrodes of the second and third transistors which serves as an output of the inverter, by measuring a current that flows through the resistor while the first transistor is kept on and the fourth transistor is kept off, and

in a case where one end of a resistor of which another end is connected to the supply voltage is connected to a node between the second electrodes of the second and third transistors which serves as the output of the inverter, by measuring a current that flows through the resistor while the fourth transistor is kept on and the first transistor is kept off.